

## Interfacing the PD243X Alphanumeric Programmable Display<sup>TM</sup> with the SAB80515/SAB80535 Microcontroller

To Produce a Bidirectional, Speed Regulated Moving Message Display by Using the SAB80515/SAB80535's Timer 2 & 8-Bit Converter

# Appnote 49

This application note introduces the user to one of the features of Timer 2 and A/D converter of the SAB 80515/535. Included in this application note is a description of both the software and hardware implementations of the SAS 80515/535 to use its Timer 2 and 8-bit A/D converter for the bidirectional, speed regulated moving message display. The program listing demonstrates how the Timer 2 and the 8-bit A/D converter of the SAB 80515/535 can be combined to generate time delays controlled by analog levels. The hardware circuitry shows an interface of the SAP 80515/535 with a simulated analog input, a 2 kbyte EPROM, and intelligent display chips of Siemens used in memory mapped 1/0 scheme.

The SAB 80515/535 microcontroller with on-chip A/D converter and a 16-bit Timer (Timer 2) with reload capability offers a solution which can be applied to a wide range of industrial applications. These applications vary from analog controlled digital delays to controlled frequency converters for pulse width modulation.

In the present application example, the above features of the SAB 80515/535 are used in conjunction to generate the software delays. The software delay results in varying the voltage level of the analog signal applied to the A/D converter of the SAB 80515/535.

## A/D Converter

The SAB 80515/535 provides an 8-bit A/D converter with eight multiplexed analog input channels on-chip. In addition, the A/D converter has a sample and hold circuit and offers the feature of software programmable reference voltages. For the conversion, the method of successive approximation with a capacitor network is used.

Figure 1 shows a block diagram of the A/D converter. There are three user-accessible special function registers:

-ADCON (A/D converter control register)

-ADDAT (A/D converter data register)

—DAPR (D/A converter program register) for the programmable reference voltages.

© 2000 Infineon Technologies Corp. • Optoelectronics Division • San Jose, CA www.infineon.com/opto • 1-888-Infineon (1-888-463-4636) OSRAM Opto Semiconductors GmbH & Co. OHG • Regensburg, Germany www.osram-os.com • +49-941-202-7178 Special function register ADCON is used to select one of the eight analog input channels to be converted, to specify a single or continuous conversion, and to check the status bit BSY which signals whether a conversion is in progress or not.

The special function register ADDAT holds the converted digital 8-bit data result. The data remains in ADDAT until it is overwritten by the next converted data. The new converted value will appear in ADDAT in the 15th machine cycle after a conversion has been started. ADDAT can be read and written to under software control. If the A/D converter of the SAB 80515/535 is not used, register ADDAT can be used as an additional general-purpose register.

The special function register DAPR is provided for programming the internal reference voltages IVAREF and IVAGND. In the present application DAPR holds a value of 00H. For this value of DAPR, IVAREF and IVAGND are the same as VAREF and VAGND respectively.

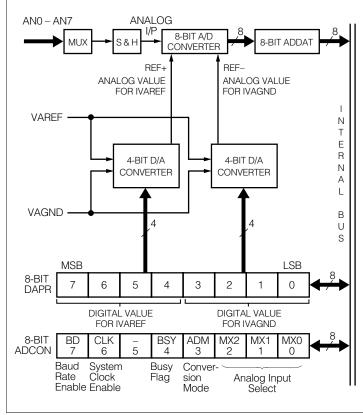
#### A/D Conversion

A conversion is started by writing to the special function register DAPR. A "Write-to-DAPR" will start a new conversion even if a conversion is currently in progress. The conversion begins with the next machine cycle. The busy flag BSY will be set in the same machine cycle as the "write-to-DAPR" operation occurs. If the value written to DAPR is 00H, meaning that no adjustment of the internal reference voltages is desired, the conversion needs 15 machine cycles to be completed. Thus, the conversion time is 15 µs for 12 MHz oscillator frequency.

After a conversion has been started by writing into the special function register DAPR, the analog voltage at the selected input channel is sampled for 5 machine cycles (5  $\mu$ s at 12 MHz oscillator frequency), which will then be held at the sampled level for the rest of the conversion time.

The external analog source must be strong enough to source the current in order to load the sample & hold capacitance, being 25 pF, within those 5 machine cycles.

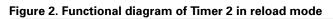
Figure 1. Block diagram of A/D converter

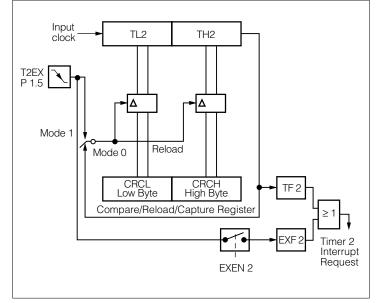


Conversion of the sampled analog voltage takes place between the 6th and 15th machine cycle after sampling has been completed. In the 15th machine cycle the converted result is moved to ADDAT.

## Timer 2

The SAB 80515 has three 16-bit Timer/Counters: Timer 0, Timer 1 and Timer 2. These Timers can be configured to operate either as





timers or event counters. Timer 2 is the time base of the programmable Timer/Counter Register Array (PTRA) unit. In addition to the operational modes "Timer" or "counter", Timer 2, being the time base for the PTRA unit, provides the features of:

- —16-bit reload
- —16-bit compare
- —16-bit capture

The reload mode of Timer 2 is used in this application to generate software delays. For explanation of the other modes please refer to the users' manual.

## Reload

The reload mode for Timer 2 is selected by bits T2R0 and T2R1 in special function register T2CON as illustrated in Table 1. In mode 0, when Timer 2 rolls over from all 1s to all 0s, it not only sets TF2 but also causes the Timer 2 registers to be loaded with the 16-bit value in the CRC (compare/reload/capture) register which is preset by software. The reload will happen in the same machine cycle in which TF2 is set, thus overwriting the count value 0000H.

Table 1. Timer 2 reloau mode selection				
T2RI	T2R0	Mode		
0	Х	Reload Disabled		
1	0	Mode 0: Auto-Reload upon Timer 2 Overflow (TF2)		
1	1	Mode 1: Reload upon Falling Edge at Pin T2EX/P1.5		

#### Table 1. Timer 2 reload mode selection

## PD2435

The PD2435 is a CMOS 4-character 5x7 dot matrix alphanumeric programmable display with ROM to decode 128 ASCII alphanumeric characters and enough RAM to store the display's complete four digit ASCII message with software programmable attributes. The CMOS IC incorporates special interface control circuitry to allow the user to control the module as a fully supported microprocessor peripheral.

## Microprocessor Interface

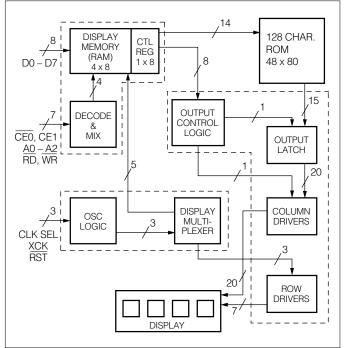
The interface to the microprocessor is through the address lines (A0-A2), the data bus (D0-D7), two chip select lines ( $\overline{CE0}$ , CE1), and ( $\overline{RD}$ ) and ( $\overline{WR}$ ) lines. The  $\overline{CE0}$  should be held low and CE1 held high when executing a read or write to a specific PD243X device. The read and write lines are both active low. A valid write will enable the data as input lines.

## Programming the PD2435

There are five registers within the PD2435. Four of the registers are used to hold the ASCII code of the four display characters. The fifth register is the Control Word, which is used to blink, blank, clear or dim the entire display to change the presentation (attributes) of individual characters.

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#### Figure 3. PD2435 block diagram showing the major blocks and internal registers



#### Application

The speed regulated moving message display is an example where a digitized value of the controlling analog signal is used to compute a reload value for the Timer 2. The Timer 2 is operated in mode 0 where this reload value becomes a starting point for the Timer to count up. On overflow the Timer automatically takes the restart value for counting from reload register CRC. While the Timer is counting up, a new reload value is computed using the present A/D value.

#### Hardware

The circuit used in this application has the advantage of requiring a minimum of components. The single chip microcomputer SAB 80535 operates in conjunction with four alphanumeric programmable display chips PD 2435 to form a 16-digit long display.

The ASCII-coded data is transferred from the SAB 80535 to the display ICs via the data port P0 and using the control signal WR (P3.6) of the SAB 80535. The address pins from the ports P0 and P2 of the SAB 80535 are used to address the EPROM as well as the display chips in a memory-mapped I/O scheme. The display chips are addressed as memory locations with the following addresses.

Display Chip	Control Register Address	Digits Address
1	1000H	1004H-1007H
2	2000H	2004H-2007H
3	4000H	4004H-4007H
4	8000H	8004H-8007H

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## **Firmware Description**

Besides controlling speed of the moving message, there is a provision to interrupt the moving message and roll it backwards to the beginning of the message. The microcontroller reads the code and the message to display from an EPROM 2716A interfaced to the ports P0 and P2 of the SAB 80535. A virtual image of the message is created in the internal RAM of the SAB 80535. Four display chips PD2435 are interfaced to the SAB 80535 in a memory-mapped scheme and can be addressed as external memory to the SAB 80535. The virtual image of the message in internal RAM of the SAB 80535 is used to manipulate data to be displayed on the display chips. The internal RAM used for the display can be viewed as an area divided into two portions:

- 1. For active display
- 2. As a data buffer

The active display area is the replica of the data being displayed on the display chips. In this case the 16-digit display would need 16 RAM locations which correspond to 16 digits currently being displayed. The data buffer contains the rest of the message which is not being displayed. The message is shifted character by character in the RAM area. When the message on the display moves from right to left, the RAM buffer acts in "First In First Out" mode, and when the message on the display moves from left to right, the data to the display from the microcontroller RAM buffer is supplied in the "Last In First Out" scheme.

Between display of every character there is a software delay which depends upon the level of the analog signal supplied to the ANO pin of the SAB 80535. The external interrupt 0 (at port P3.2) is used to interrupt the microcontroller to inform it that the message needs to be scrolled backwards. On getting this interrupt the software sets the flag bit 0 which remains set until the message is scrolled back to the beginning of the message.

#### List of Components

Name	Number
SAB 80535	1
271 6A	1
PD2435	4
12 MHz Crystal	1
74LS373	1
22 pF Capacitors	2
100 nF Capacitor	1
4.7 μf Capacitor	1
1 k Resistor	1
10 k Pot	1

#### **Reference Material for ICs**

1. SAB 80515/80535 User's Manual.

2. PD2435 Data-Sheet or Optoelectronic Data Book (1990).

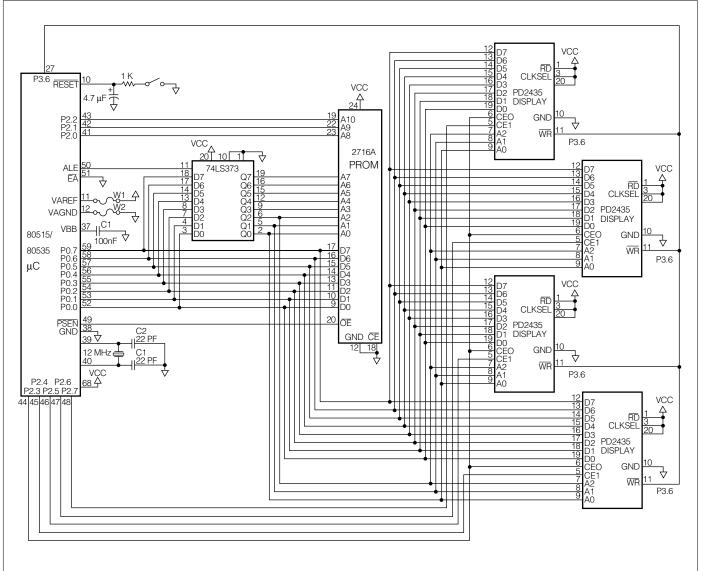
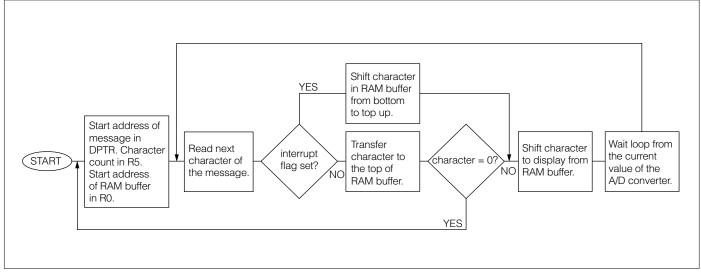


Figure 5. Program flow chart



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#### **Program listing**

UDISP	'PD 2435 Display PROGRAM'					
	1 2 3 4	\$TITLE ('PD \$MOD515 \$NOSYMB(		PLAY PROGRAM')		
	5 6 7	CSEG \$DEBUG				
0000	8 9		ORG	00H		
0000 02000C	10 11 12		LJMP	BEGIN	;Jump on reset	
	13 14 15				outine for INTO. This is used to set a flag t the message needs to be rolled back.	
	16 17 18					
0003	19 20		ORG	03H		
0003 C0E0 0005 D2D5 0007 D0E0 0009 C289 000B 32	21 22 23 24 25		PUSH SETB POP CLR RETI	ACC F0 ACC IE0	;Set flag for external interrupt	
0008 32	26 27			N PROGRAM		
	28 29 30		;			
000C D282 000E 758110	31 32	BEGIN:	SETB MOV	P3.2 SP,#10H	;Set bit for INT0	
0011 75D800	33 34		MOV	ADCON, #00H	;Select analog channel 0	
0014 C2D5 0016 7800 0018 79FF	35 36 37	OPTS:	CLR MOV MOV	F0 R3,#00H R1,#0FFH	;Clear flag 0 ;Character pointer in the message ;R1 used as a flag	
001A 90F000 001D 7403 001F F0	38 39 40		MOV MOV MOVX	DPTR,#0F000H A,#03H @DPTR,A	;Control register of all displays ;Control word for display	
0020 9000C2 0023 7820 0025 7D65	41 42 43		MOV MOV MOV	DPTR,#(TEXT-1) R0,#20H R5,#101	;Beginning of the text ;Internal RAM location ;A count for 101 characters	
0027 7420 0029 F6 002A 08 002B DDFC	44 45 46 47	BLANK:	MOV MOV INC DJNZ	A,#20H @R0,A R0 R5, BLANK	;ASCII for space ;Fill all locations with blank	
002D 12006C 0030 20D501 0033 0B	48 49 50 51	SHIF:	CALL JB INC	NEXTC F0,TEMP R3	;Read the next character ;Check if the interrupt was raised	
0033 0B 0034 7D65 0036 7820 0038 20D506	51 52 53 54	TEMP:	MOV MOV JB	R5,#101 R0,#20H F0,REV0	;If no interrupt ;Character count in message ;RAM location 20H	
0038 20D508 003B C6 003C 08 003D DDFC	54 55 56 57	SHFT:	XCH INC DJNZ	A,@R0 R0	;If no interrupt ;Add the character :To the top of the BAM buffer	
003F 0158 0041 7421	58 59	REV0:	AJMP MOV	R5,SHFT CONT0 A,#21H	;To the top of the RAM buffer ;If there is no interrupt	
0043 2B	60		ADD	A,R3	;Offset for the RAM buffer	

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0044 F8 0045 7600 0047 7820 0049 E6 004A C0E0 004C 08 004D E6 004E 18 004F F6 0050 08 0051 DDF9 0053 08 0054 7600 0056 D0E0 0058 7820 005A E9 005B 6087 005D 120071 0060 C2AF 0062 1200A4 0065 75A881 0068 D288 006A 012D	61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84	AGAIN: CONT0:	MOV MOV MOV PUSH INC MOV DEC MOV INC DJNZ INC MOV POP MOV MOV JZ CALL CLR CALL CLR CALL MOV SETB AJMP	R0,A @R0,#00H R0,#20H A,@R0 ACC R0 A,@R0 R0 @R0,A R0 R5,AGAIN R0 @R0,#00H ACC R0,#20H A,R1 OPTS OUTC IEN0.7 WAITA IEN0,#81H IT0 SHIF	<ul> <li>Pointer in the RAM buffer</li> <li>Displayed so far</li> <li>Beginning of the RAM buffer</li> <li>Read the character</li> <li>Save it</li> <li>Next location in RAM buffer</li> <li>Read the next character</li> <li>Back to first character</li> <li>Back to first character</li> <li>Replace with second character</li> <li>Process repeats</li> <li>Moving character buffer</li> <li>Restore character</li> <li>Beginning of character buffer</li> <li>Check if end of character buffer</li> <li>Check if end of character buffer</li> <li>Enable interrupt</li> <li>INT0 control bit</li> </ul>
	85 86		; The	routine moves a ch	aracter of the message to ACC.
	87				
006C A3	88 89	NEXTC:	INC	DPTR	
006C A3 006D 7400 006F 93 0070 22	90 91 92 93	NEXTC.	MOV MOVC RET	A,#0 A,@A+DPTR	;Move the character to Acc.
	94 95		; — This	routine displays and	d moves a character over the four digits of
	96				peats for the next display chip and so on.
	97		;		
	98 99		,		
0071 C0E0	100	OUTC:	PUSH	ACC	
0073 C082 0075 C083	101 102		PUSH PUSH	DPL DPH	
0077 7A04	102		MOV	R2,#4	;For four digits (0 to 3) in a chip
0079 901004	104		MOV	DPTR,#1004H	;Digit 0 in first display chip
007C 120098 007F 902004	105 106		CALL MOV	OUTC0 DPTR,#2004H	;Digit 0 in second display chip
0082 120098	107		CALL	OUTC0	
0085 904004	108		MOV CALL	DPTR,#4004H	;Digit 0 in third display chip
0088 120098 008B 908004	109 110		MOV	OUTC0 DPTR,#8004H	;Digit 0 in fourth display chip
008E 120098	111		CALL	OUTCO	
0091 D083	112		POP	DPH	
0093 0082 0095 D0E0	113 114		POP POP	DPL ACC	
0095 0020	114		RET		
	116				
	117		; — Thia	is a neeted subrout	tine. It moves a nonzero hex value (ASCII)
	118 119			left to right of the	
	120				<u> </u>
	121		, ,		
	122	<b>A</b> 1 <b>-</b>			
0098 E6	123	OUTC0:	MOV	A,@R0	

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0099 6007 0098 F0 009C 08 009D A3 009E DAF8 00A0 7A04 00A2 F9 00A3 22	124 125 126 127 128 129 130 FIN: 131 132 133	FIN:	JZ MOVX INC DJNZ MOV MOV RET ; This	FIN @DPTR,A R0 DPTR R2,OUTC0 R2,#4 R1,A	es the software delay. The delay is
134 135 136 137 138			. gene	erated by the timer 2	2. The start count of the timer 2 is ent value of the A/D converter.
00A4 7E03 00A6 7D10 00A8 75DA00 00AB E5D9 00AD 75F0FF 00B0 A4 00B1 F5CA 00B3 85F0C8 00B6 75C811 00B9 10C602 00BC 01B9 00BE DDE8 00C0 DEE4 00C2 22	139 140 141 142 143 144 145 146 147 148 149 150 151 152 153 154	WAITA: WAITB: WAITC: WAITD: WAITE:	MOV MOV MOV MOV MUL MOV MOV MOV JBC AJMP DJNZ DJNZ RET	R6,#03H R5,#10H DAPR,#00H A,ADDAT B,#255 AB CRCL,A CRCL,A CRCH,B T2CON,#11H TF2,WAITE WAITD R5,WAITC R6,WAITB	;For computing reload value ;Reload value is computed ;Load the reload value low ;Load the reload value high
	154 155 156 157		; MES	SAGE	
00C3 20202020 00C7 20202020 00CB 20202020 00CF 20202020	158 159	TEXT:	DB		,
00CF 20202020 00D3 5349454D 00D7 454E5320 00D8 4D494352 00DF 4F434F4E 00E3 54524F4C 00E7 4C455220 00EB 53414220 00EF 38303531 00F3 352F3533 00F7 35	160		DB	'SIEMENS MICRC	OCONTROLLER SAB 80515/535'
00F8 20202020 00FC 20202020 0100 20202020 0104 53414220 0108 38303531 010C 352F3533 0110 35202020 0114 20202020 0118 20202020 011C 20202020	161		DB	' SAB 80515	5/535 ',0
0120 00	162		END		

### ASSEMBLY COMPLETE, 0 ERRORS FOUND